

SEBASTIAN P. SHOLL

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SUMMARY

Hardware designer with expertise in high-end ASIC methodology and design. Experienced in delivering tools, flows and design automation to enable reliable tapeout ready designs. Looking for new opportunities to broaden skills and knowledge across the semiconductor industry.

PROFESSIONAL EXPERIENCE

Apple, Austin, TX

Dec 2017 - Present

Top Level Physical Design Engineer (2017-Present)

Intel, Edina, MN and Hudson, MA

May 2012 - Nov 2017

Senior Hardware Engineer (2014-Present)

- Interfaced with central design automation and cross organizational teams to integrate converged tools and flows into the Omnipath second generation environment. Deployed two physical design environments used by cross-site teams across three Omnipath ASICs.
- Developed a verification environment for centralized signoff of blocks and full chip designs. Centralized environment provided a “known good” configuration for block and full chip signoff, decreasing time needed for chip convergence.
- Execution owner for chassis block on the second generation Omnipath ASIC. Integration of multiple SIPs and HIPs delivered from across the organization. Extremely challenging design with regards to proper constraint, clocking and physical layout required.
- Member of the tapeout team for first generation Omnipath ASICs. Drove block and full chip LVS, DRC, ERC and Antenna closure. Developed methods to systematically resolve issues, allowing for correct by construction, quick RTL to GDS and ECO turns.
- Promoted best known practices throughout the design team by championing project and flow documentation. Provided frequent training to the physical design team and acted as a mentor for junior engineers.

Hardware Engineer (2012-2013)

- Execution owner for two large hierarchical blocks in the first generation Omnipath Switch ASIC.
- Lead back end tools, flows and methodologies for Omnipath ASICs. Directed meetings, created task lists, tracked progress and drove methodology across the physical design team.
- Designed and deployed a methodology to generate physical design kits for multiple ASICs. Integrated IP deliveries from IP providers for use by logic, verification and physical design teams.
- Managed design databases and collateral for multiple ASICs with a custom design repository tool. Supported both top down and bottoms up hierarchical methodologies. Introduced contouring to handle interface changes and decrease time for full chip model builds.
- Worked closely with IT to maintain and deploy wiki, SharePoint, bug tracking, compute and disk resources for the Omnipath organization.
- Pushed physical design quality checks earlier into the logic design development process to help enable a constant integration handoff model between front and back end.

Cray Inc, Eau Claire, WI

Apr 2007 - May 2012

Hardware Engineer (2011-2012)

- Back end flow developer for Pisces 28nm NIC ASIC. Deployed multi corner multi mode synthesis and automatic place and route flows.
- Responsible for integration of internal and external HIPs within the back end design environment. Drove

resolution of library issues with HIP providers. Put in place automation to generate tool design views and validate quality of delivered HIP.

- Devised a configuration management and revision control environment for release of tools and libraries across the back end design environment.
- Developed a front end synthesis and basic floorplanning flow for use by the Pisces logic design team.

Design for Test Engineer (2007-2011)

- Worked on multiple generations of ASIC routers. Gemini a 90nm 48-port 44M gate Router and Aries a 40nm 217M gate 48-port Router.
- Execution owner for Aries DFT and TAP blocks. Developed and debugged scan and MBIST insertion scripting for Aries
- Owner for DFT linting across the whole of Aries and Gemini designs. Worked closely with logic designers to resolve DFT issues impacting testability and scan test coverage.
- Assisted STA team to resolve block and full chip DFT timing issues.
- Developed a simulation environment used for creation and debug of wafer and package tests. Testing included HT3, MBIST, PLL, JTAG and PCIE Gen3.
- Collaborated with external test team to bring manufacturing tests to production. Resolved DFT power consumption issues for MBIST through targeted testing of individual cores.

EDUCATION

University of Wisconsin-Platteville, Platteville WI

Bachelor of Science, December 2006

Major: Electrical Engineering

Emphasis: Computer Engineering, Power and Energy Distribution

- Eta Kappa Nu Electrical Engineering Honor Society, UW-Platteville: Inducted Spring 2003
- Tau Beta Pi National Engineering Honor Society, UW-Platteville: Inducted Spring 2003

TOOLS & PROGRAMMING SKILLS

- *Software:* Synopsys Tools, Design Compiler, IC Compiler, PrimeTime, Spyglass, Formality, TetraMAX, VCS, IC validator, Cadence Innovus, Mentor Calibre.
- *Revision control:* Git, Perforce
- *Programming:* Perl, Tcl/Tk, SQL, Unix, XML, XHTML
- *HDL Languages:* System Verilog, Verilog